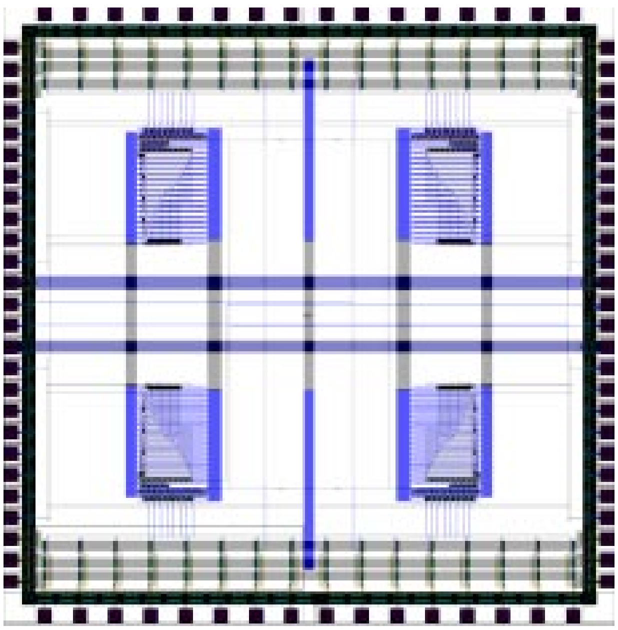
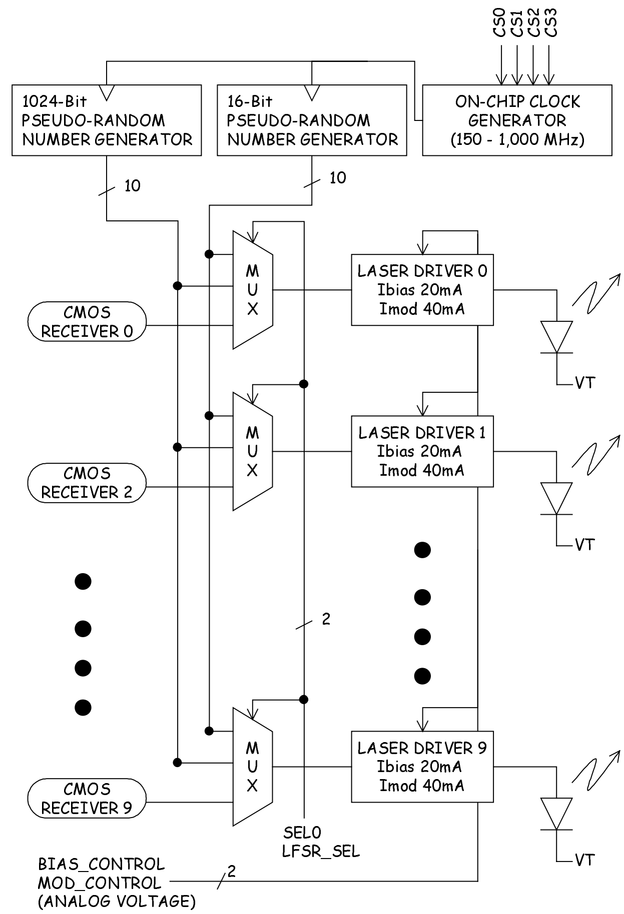
CLDA2: A 500Mb/s, 32-Channel CMOS Laser Diode Array Driver with built-in self-test and clock generator circuitry

Chip Specification





FEATURES:

- 0.5 micron HP14TB CMOS
- 4.4mm x 4.4mm 84-pad chip
- 3.3V or 5V Supply voltage
- 50,000 MOS transistors
- Adjustable bias (0-10mA)
- Adjustable modulation (0-20mA)
- Industry standard 250μm output pad pitch in a 16x1 double-row configuration.
- Modes of operation: Self-test mode or asynchronous 32-channel driver mode
- 8 On-chip pseudo random # generators provide data patterns in self-test mode
- 16 on-chip high-speed clock generators (100-500 MHz) in self-test mode
- Max. 500Mbit/sec/channel in self-test mode
- Max. 150Mbit/sec/channel in normal mode (limited by CMOS IO driver speed)
- Proven circuit design (the driver circuit was used in the 1997 JOP-OIDA run)
- Packaging: bare die or 84-pin PGA

Designer: Fouad Kiamilev (kiamilev@uncc.edu)

Overview

The CLDA2 chip is a powerful tool for operating vertical cavity surface emitting laser (VCSEL) device arrays. It can function as an asynchronous 32-channel driver with 32 CMOS-level inputs and 32 current-mode outputs. Modulation and bias are adjustable over a wide range (20mA for bias and 40mA for modulation). The CLDA chip is unique because it can also operate in self-test mode. In this mode, a pseudo-random data stream is generated on-chip and transmitted to the VCSEL array. An adjustable on-chip clock generator (150MHz to 500MHz) is used to synchronize the operation (in self-test mode). Thus, the CLDA2 chip can test high-speed operation of VCSEL device array without requiring high-speed signal generation equipment. For device researchers, systems designers and users of VCSEL array devices, the CLDA2 chip provides a simple and effective method to test high-speed performance of their array devices.

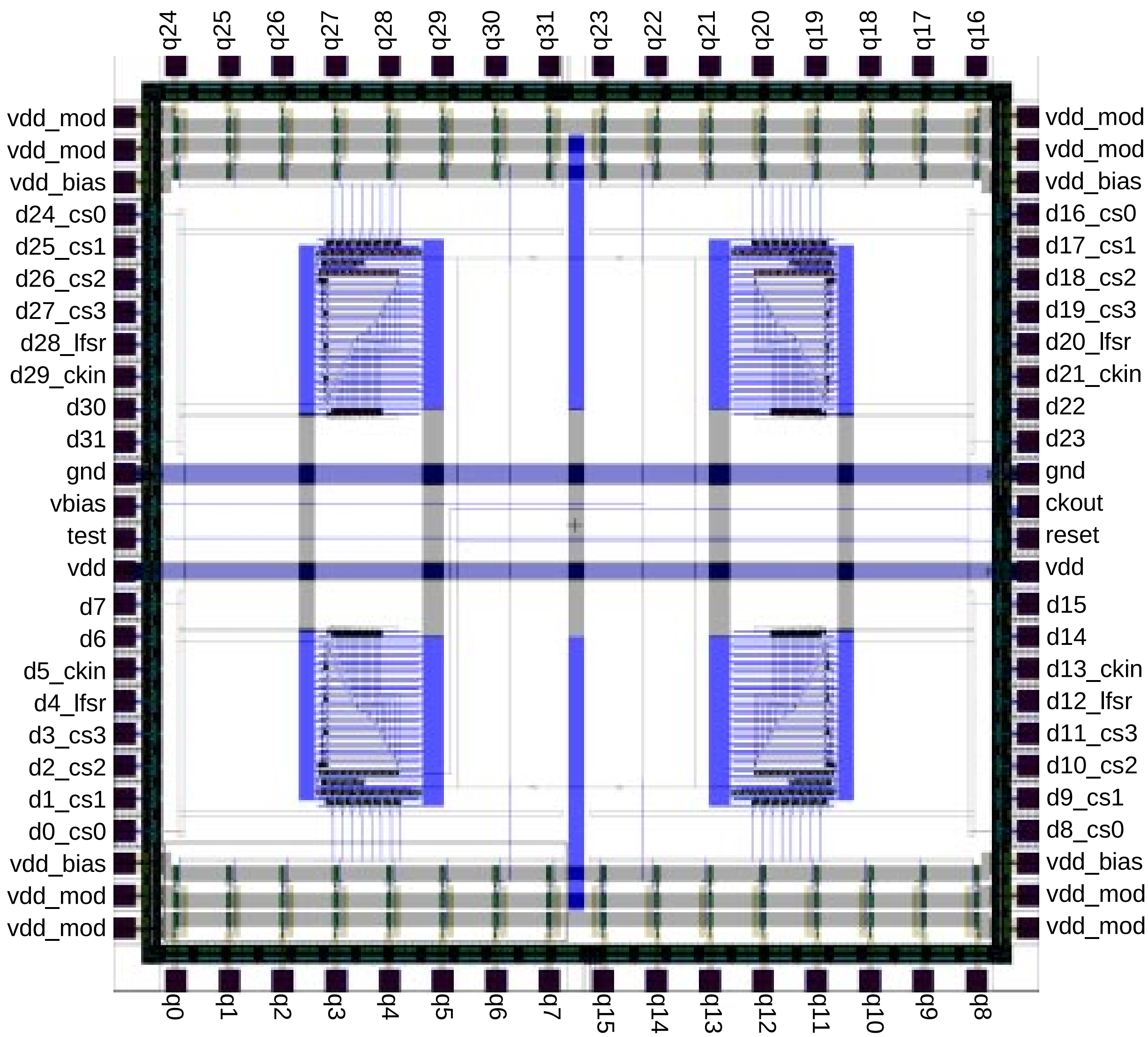


Figure 1: CLDA pins-out diagram. Output pads to drive the laser diodes are spaced 250µm apart along the north and south sides of the chip. The east and west sides of the chip have input pads and power supply connections for laser diode drivers.

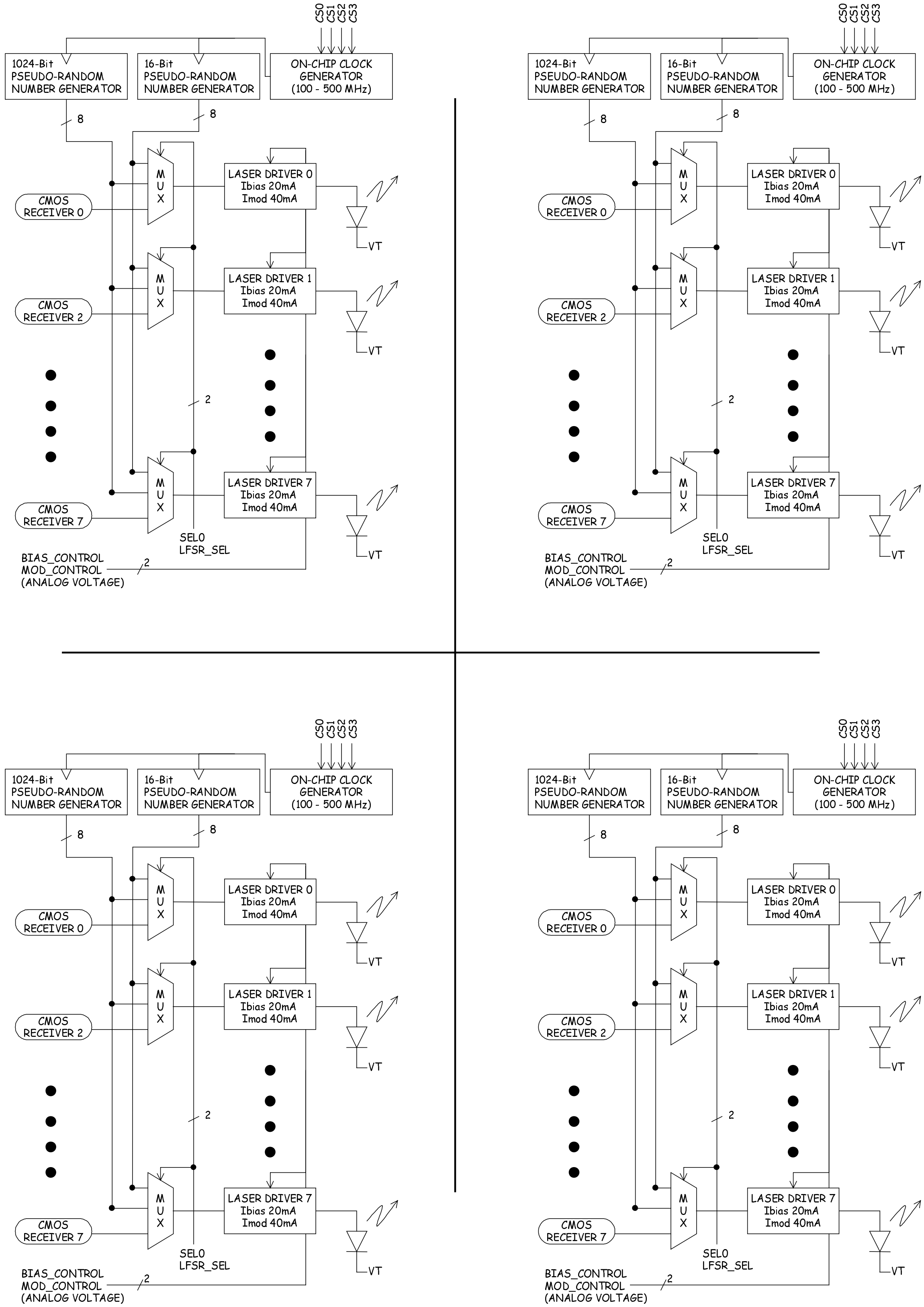


Figure 2: CLDA2 block diagram. The chip is partitioned into 4 8-channel driver blocks.

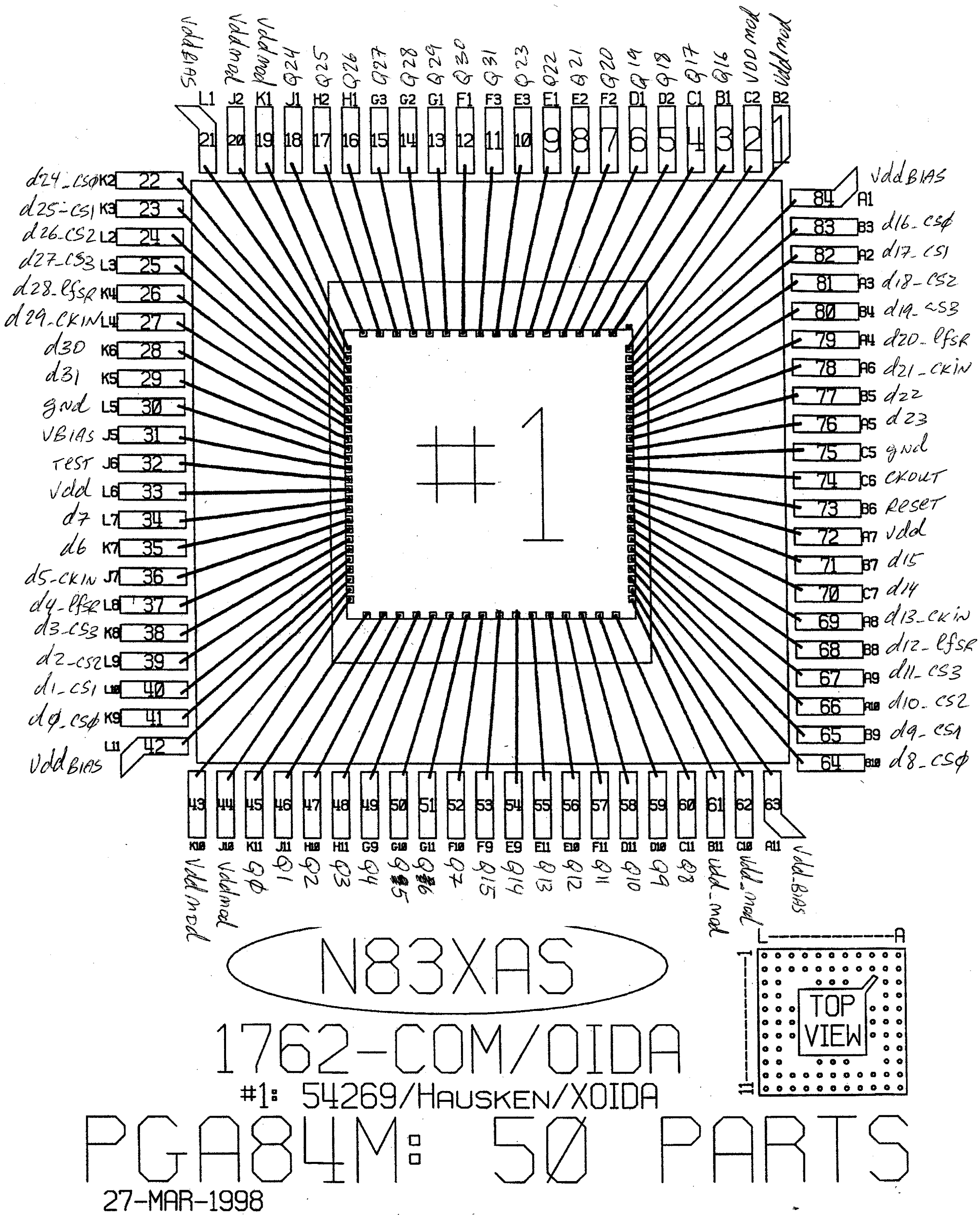


Figure 3: CLDA2 wire-bonding diagram for 84-pin PGA package.

Pin Description

Name	Description
D0-D31	INPUT-CMOS. When chip is operated in *asynchronous driver mode*, parallel data on this bus is asynchronously transmitted to the VCSEL drivers. The inputs are inverted (a “1” input to D0 produces 0mA modulation current output on Q0). When the chip is operated in *self-test mode*, some of the D0-D31 pins are used to configure the clock speed and test data pattern. For example, the D20_LFSR pin in figure 1, functions as input D20 in *asynchronous driver mode*. In *self-test mode*, this pin selects the pseudo-random number pattern that is generated on chip (and transmitted on Q16-Q23).
Q0-Q31	OUTPUT-CURRENT. These output pads connect to the VCSEL device array. The CLDA chip is designed to source current, thus connection must be to the anode of the VCSEL device. To obtain maximum modulation and bias levels, the user should bias the common cathode terminal of the VCSEL device array such that the anode is at ground (0 volt) during normal device operation. Inductance on these pins (such as long wire-bonds) must be avoided, as it can lead to substantial signal degradation.
VDD_MOD	Four (8) pins are provided for power supply that controls modulation level. When set at 3.3 volts, maximum modulation of 40mA results. Reducing VDD_MOD results in smaller modulation current. To avoid electromigration and ground-bounce problems, all four pins must be connected to a low impedance, properly bypassed, adjustable power supply.
GND_MOD	Connect to ground.
VDD_BIAS	Two options: 1) Short to VDD_MOD supply or 2) Connect to a separate power supply. ***For case 2, it is necessary to put an external diode in series with the VDD_BIAS supply to prevent “floating” VDD_BIAS against VDD_MOD supply.***
GND_BIAS	Connect to ground.
VBIAS	INPUT-ANALOG. This is an analog voltage (0-3.3 volt) to control the bias level. When set at 3.3 volt, maximum bias of results. Reducing VBIAS results in smaller bias current. This input does not draw current, and can be set with a low-cost adjustable potentiometer.
RESET	INPUT-CMOS. This active low signal is used to initialize the pseudo-random number generation circuits when chip is operated in *self-test mode*. In order to properly initialize the circuitry, the chip must be powered-on with the reset asserted (e.g. set RESET low at power-on).
Dx_CS0, Dx_CS1, Dx_CS2, Dx_CS3	INPUT-CMOS. Used in *self-test mode*. Four bit nibble to select on-chip clock generator speed (CS0 is the LSB). When set to 0000, chip clock is obtained from CLKIN pin (see below). When set to 0110, 500MHz clock speed is obtained. When set to 1111, a 100MHz clock speed is obtained. Values in between will produce appropriately scaled clock speeds. Although it is possible to set 1GHZ clock speed (value of 0000), the chip will not operate at this speed. D0_CS0…D3_CS3 – select clock speed for outputs Q0…Q7 D8_CS0…D11_CS3 – select clock speed for outputs Q8…Q15 D16_CS0…D18_CS3– select clock speed for outputs Q16…Q23

	D24_CS0…D27_CS3– select clock speed for outputs Q24…Q31
Dx_CKIN	INPUT-CMOS. Used in *self-test mode*. When the appropriate CS0-CS3 nibble is set to 0000, this input provides the clock signal for synchronizing the operation of the chip. D5_CKIN – clock input for outputs Q0…Q7 D13_CKIN – clock input for outputs Q8…Q15 D21_CKIN – clock input for outputs Q16…Q23 D29_CKIN – clock input for outputs Q24…Q31
CLKOUT	OUTPUT-CMOS. This output signal contains the on-chip clock signal divided by 1024. Thus, when chip is running at 500MHZ, this output contains a 0.5MHZ clock signal. The purpose of this signal is to provide a quick and simple way to find the on-chip clock speed. This output monitors the speed of the first clock generator circuit (whose speed is set by D0_CS0…D3_CS3).
Dx_LFSR	INPUT-CMOS. Used in *self-test mode*. When set to 0, the 16-bit pseudo-random number generator circuit is used. That means that the transmitted data repeats after every 15 bits. When set to 1, the 1024-bit pseudo-random number generator circuit is used. In this case, the length of the random sequence is 1023 bits. Note that all the channels transmit the same random sequence, but it is shifted in time. D4_LFSR – select data pattern for Q0…Q7 D12_LFSR – select data pattern for Q8…Q15 D20_LFSR – select data pattern for Q16…Q23 D28_LFSR – select data pattern for Q24…Q31
VDD_DIG	Connect to 3.3 or 5.0 volt.
GND_DIG	Connect to ground.
TEST	INPUT-CMOS. When set to 0, the chip operates in *asynchronous driver mode*. When set to 1, the chip operates in *self-test mode*.

Chip Operation (Asynchronous Driver Mode)

To operate the chip in asynchronous driver mode, set both TEST and RESET to 0. Then, parallel data on the input bus (D0…D31) is asynchronously transmitted to the current-mode output bus (Q0…Q31). Modulation and bias for the current-mode output is controlled by VDD_MOD, VDD_BIAS and VBIAS pins (see Pin Description section).

Chip Operation (Self-Test Mode)

In self-test mode, the input pins (D0 through D31) are unused, while the 32 output pins (Q0 through Q31) are divided into four 8-channel blocks (Q0-Q7, Q8-Q15, Q16-Q23, Q24-Q31). Each block can then be operated independently (e.g. with different clock speed and transmit data pattern). As detailed in the *Pin Description* section, some of the unused input pins are then used to configure the clock speed and transmit data pattern for each block.

To operate the chip in self-test mode, set TEST to 1 and RESET to 0 prior to power-on. After power-on, RESET can be asserted to 1. After power-on, set Dx_LFSR to select the random sequence for each 8-channel block. Also select on-chip frequency for each block using the Dx_CSx input pins. After toggling the reset line, the current-mode output bus should be driven with a high-speed random data stream. In this mode, it is important that the chip is powered on with the RESET line tied LOW to ensure that the internal digital circuits are properly initialized at chip power-on.

Simulation Results

Extensive full-chip, spice-level simulation of the entire chip was performed. The simulation deck was created by extracting the entire chip with layout parasitic parameters such as wire capacitance and diffusion capacitance for MOSFET devices.

Over 24 hours were logged simulating the chip on a high-end SUN ULTRA workstation (simulation of 200 nanoseconds requires several hours of CPU time). Some of the results are shown on the following pages.

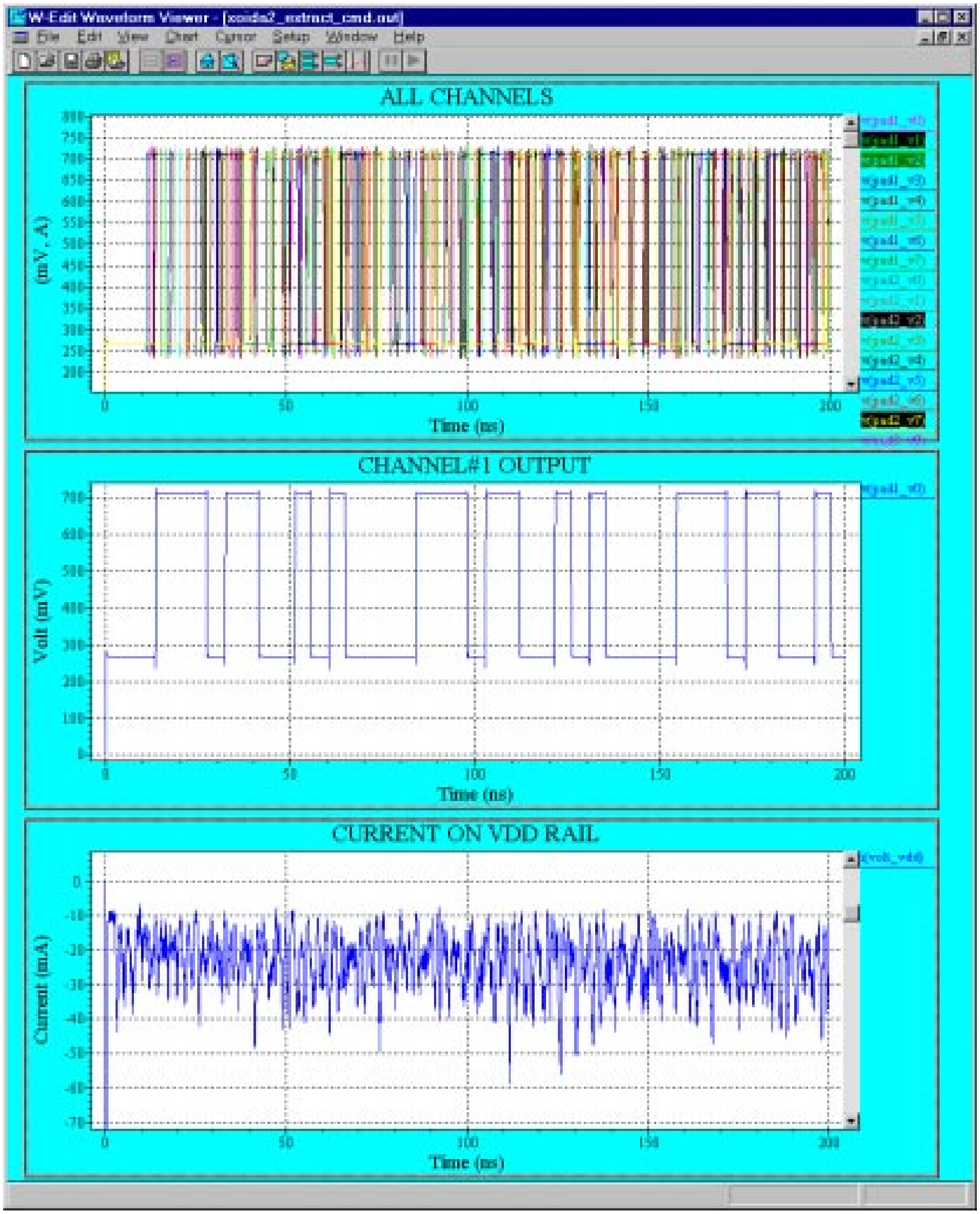


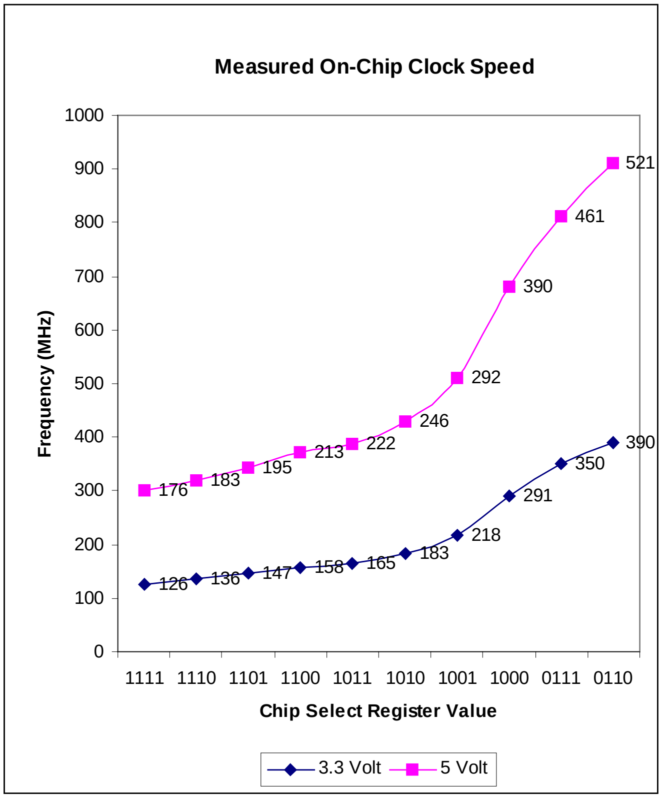
Figure 4. Self-test mode of operation is used. The on-chip clock is 200MHz and a 1024-bit random sequence is being used. The top two graphs show the output of all 32 channels superimposed (4mA bias and 8mA modulation). Middle graph shows channel 1 output. The bottom graph shows AC current on VDD power supply.

Test Results

The CLDA2 chip was fully tested and found to have identical performance (within 5%) to the 1st generation part (the 10-channel CLDA driver fabricated by OIDA in 1997). Thus the test results and circuit description below are taken from the CLDA chip. The CLDA chip was measured using the test fixture described in the previous section and found to be fully operational. The following table summarizes the performance of the chip:

Power Supply	**3.3v Supply**	**5.0v Supply**
Speed	400MHz	500MHz
Max. Bias Current	10mA	20mA
Max. Modulation Current	20mA	40mA

The performance of the on-chip clock generator circuit was measured (see figure 5). Note that the on-chip clock generator fails to operate for CS values higher than 0110, due to on-chip parasitic capacitance in the digital portion of the chip. Note that changing the supply voltage can make small adjustments in the on-chip clock frequency.



Measured Speed for On-Chip Clock Generator

CS3	CS2	CS1	CS0	Measured Frequency (MHz) 3.3v Supply	Measured Frequency (MHz) 5v Supply
1	1	1	1	126	176
1	1	1	0	136	183
1	1	0	1	147	195
1	1	0	0	158	213
1	0	1	1	165	222
1	0	1	0	183	246
1	0	0	1	218	292
1	0	0	0	291	390
0	1	1	1	350	461
0	1	1	0	390	521

Figure 5. Measured characteristic of the on-chip clock generator.

Low-speed test measurements of the CLDA chip were performed using a 10MHz TTL clock IC as the clock source for the self-test circuitry on the CLDA die. The data was taken with all 10 channels transmitting 16-bit PRBS data stream at full speed (see figure 10). In this measurement, VCSEL devices were “emulated” using 50Ω 0805 surface mount resistors terminated to ground. One of the ten drivers was connected using a 50Ω SMA cable to a high-speed digital oscilloscope with 50Ω DC terminated input. High-speed measurements were performed using an on-chip clock generator. Using a 5volt supply and a CS register setting of 0110, a 521Mbit/sec data stream was obtained at the output of CLDA chip (see figure 6). The setup for this measurement was identical to the 10MHz measurement. Note that the “noise” in the high-speed measurement is due to the parasitic inductance of the PGA package and impedance mismatches along the 50Ω transmission line.

DC performance of the CLDA chip was also measured and is discussed in the next section. In that section, we also describe the circuit topology of the VCSEL driver circuit used on the CLDA chip. This is done in order to provide the user with a “feel” on how to configure the CLDA chip for use in their own systems.

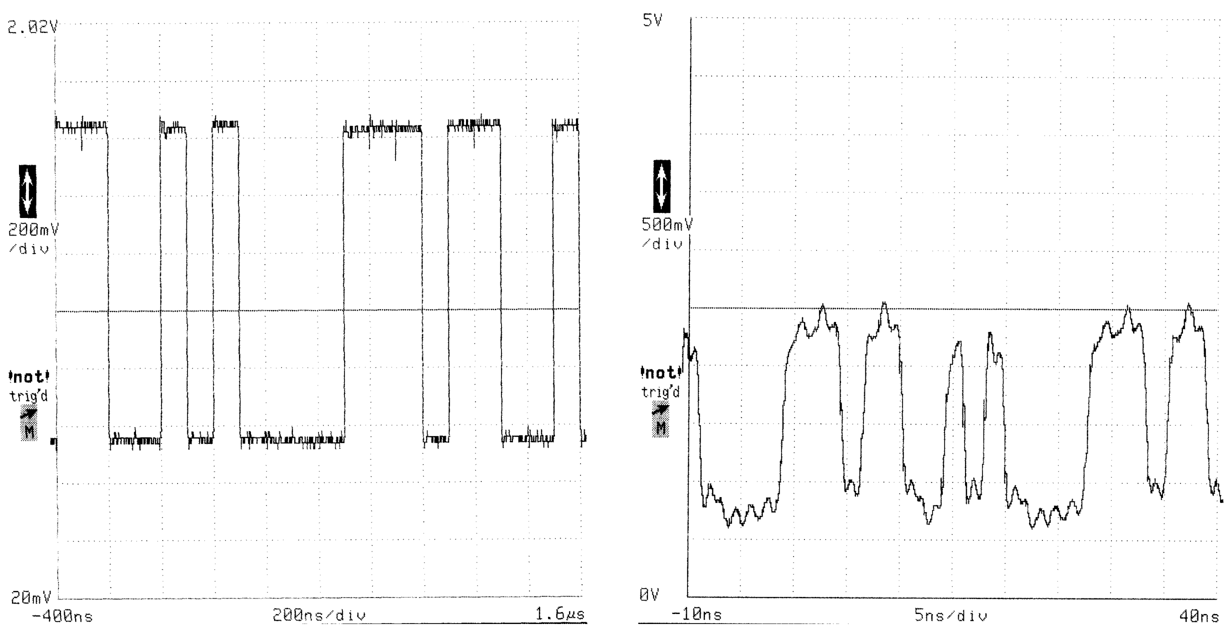


Figure 6: Measured performance of the CLDA VCSEL driver circuit. Operation at 10MHz is shown on the left side. Operation at 500MHz is shown on the right side.

VCSEL Driver Circuit

The CLDA VCSEL driver circuit is designed to source current. It consists of two PMOS drain-shorted transistors that are designed to source current while operating in saturation regime. Figure 7 shows the layout and logic schematic for the circuit. Note that the VCSEL device is shown as a 50Ω resistor in parallel with 250fF of capacitance. However, typical, VCSEL devices operate with a DC turn-on voltage of 1.5-2.5 volts (herein called VT). Thus, we recommend that when using this driver, the N-side of the VCSEL be tied to approximately –VT voltage. If the N-side of the VCSEL is tied to ground, then the bias and modulation currents will be reduced (from the measured data). If you have to use N-side grounded VCSEL devices, we recommend operating the circuit with 5v supplies. The following paragraphs explain the operation of the CLDA driver circuit.

The circuit operates on a simple principle that a MOS transistor in saturation acts as a current source. It consists of two drain-shorted transistors: M1 supplies the modulation current, and M2 supplies the bias current. The drain of M2 is connected to the power supply rail (either 3.3v or 5.0v). The gate of M2 is connected to an analog voltage that sets the bias current (herein called VBIAS). Figure 8 shows the measured dependence of bias current and VBIAS. Note that increasing VBIAS voltage, reduces bias current. Thus VBIAS set 0v produces maximum bias current.

Transistor M1 controls the modulation current. The gate of M1 is connected to a digital input signal with 3.3v or 5.0v swing. The source of M1 is connected to a power supply, VMOD, which controls the modulation current. By raising the VMOD voltage, we increase the modulation current (and vice-versa). Figure 9 shows the dependence of the modulation current on VMOD. It is important to point out that a buffer must be used to drive the gate of M1, since it is a big transistor with a large gate capacitance. Spice simulations with extracted layout should be used to determine the appropriate buffering to achieve the desired operating speed.

When using the CLDA chip in your systems, it is critical that GND, VMOD and VDD power supplies (connected to sources of M1 and M2 respectively) are properly de-coupled using high-quality surface mount capacitors and (in case of VMOD and GND) connected to solid planes on the PCB.

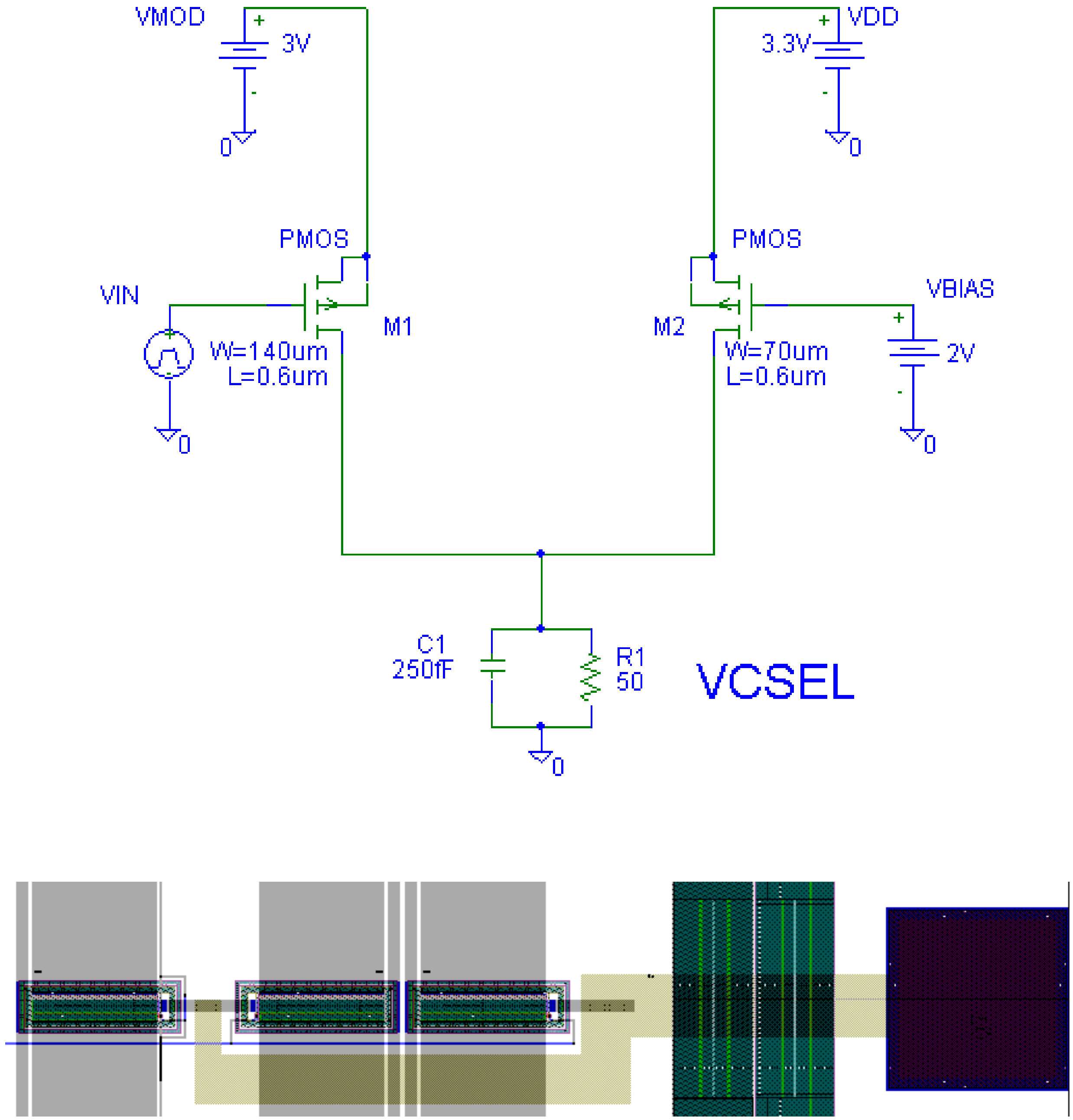
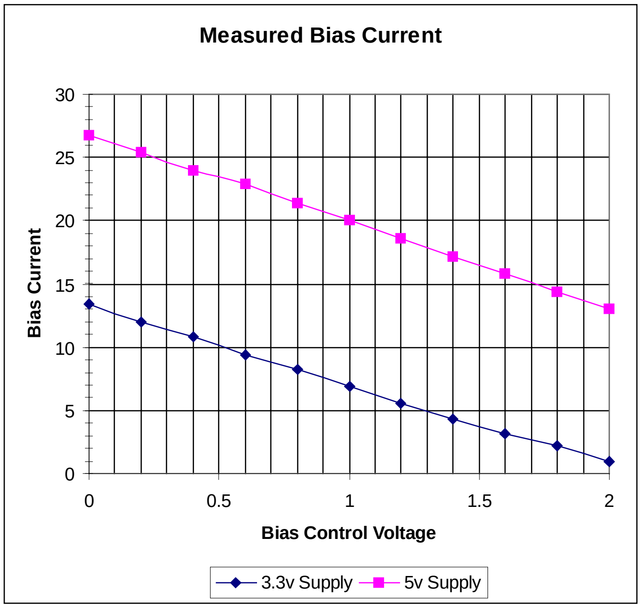


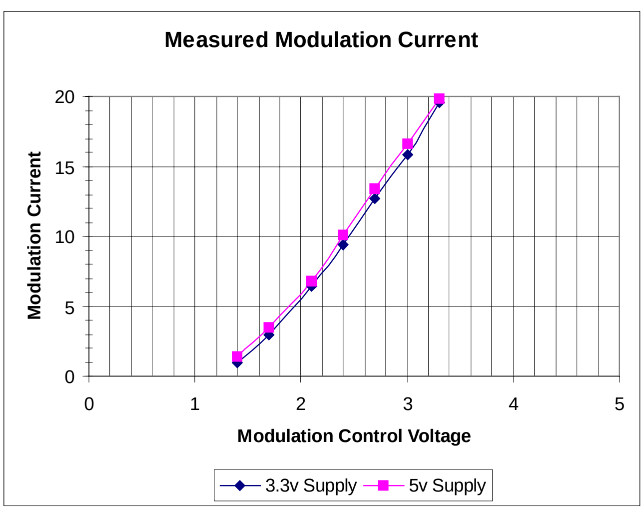
Figure 7. Schematic and layout for ODIA-CLDA VCSEL driver circuit. Note that the layout includes an output pad.



Measured Bias Current Drive

Vbias Control Voltage (Volts)	Measured Bias Current (mA) 3.3v Supply	Measured Bias Current (mA) 5v Supply
0	13.4	26.7
0.2	12	25.4
0.4	10.8	24
0.6	9.4	22.9
0.8	8.2	21.4
1	6.9	20
1.2	5.6	18.6
1.4	4.3	17.2
1.6	3.2	15.8
1.8	2.2	14.4
2	1	13

Figure 8. Measured bias current vs. bias control voltage (VBIAS). The measurement was done using a 50Ω connected to ground (see schematic in figure 2). To make this measurement, the modulation current driver (M1) was turned-off.



Measured Modulation Current Drive

Vmod Supply Voltage (Volts)	Measured Modulation Current (mA) 3.3v Supply	Measured Modulation Current (mA) 5v Supply
1.4	1	1.4
1.7	3	3.5
2.1	6.4	6.8
2.4	9.4	10.1
2.7	12.7	13.4
3	15.8	16.6
3.3	19.6	19.8

Figure 9. Measured modulation current vs. modulation power supply voltage (VMOD). The measurement was done using a 50Ω connected to ground (see schematic in figure 2). To make this measurement, the bias current driver (M2) was turned off. To obtain 40mA modulation current, raise VMOD supply to about 5 volts (measured data goes up to 3.3v only).